FPGA
FPGA.SchDoc

PowerSupply
PowerSupply.SchDoc

IO
IO.SchDoc

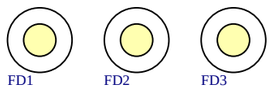
Peripherals
Peripherals.SchDoc

Memory_Expansion
Memory_Expansion.SchDoc

Displays
Displays.SchDoc

Expansion_Buffers
Expansion_Buffers.SchDoc

Board Fiducials



Variant	Description	Rev	Notes
V3	Plus & Accelerated	3.4	Final

SpectrumNext

Overview

Drawn By:

Project #: PR0064 | Rev: 3.4 | Variant : V3 | Sheet: 1 of 8

SpecNext Ltd

FPGA

U1B

+1.8V	K12	VCCAUX
	H12	VCCAUX
	M12	VCCAUX
	F12	VCCAUX
+1.0V	F10	VCCBRAM
	G11	VCCBRAM
	N9	VCCINT
	F8	VCCINT
	G9	VCCINT
	N11	VCCINT
	M10	VCCINT
	H8	VCCINT
	N7	VCCINT
	G7	VCCINT
	M8	VCCINT
	L11	VCCINT
	J11	VCCINT
	L7	VCCINT
	K8	VCCINT
+1.8V_ADC	J7	VCCINT
	H10	VCCADC 0
	E8	VCCBATT 0
GND	J9	VREFN 0
	K10	VREFP 0
A_GND	R9	VCCO 0
	T12	VCCO 14
	V18	VCCO 14
	P16	VCCO 14
	L17	VCCO 14
	N13	VCCO 14
	U15	VCCO 14
	A17	VCCO 15
	D16	VCCO 15
	G15	VCCO 15
	C13	VCCO 15
	H18	VCCO 15
	K14	VCCO 15
	B10	VCCO 16
	V8	VCCO 34
	U5	VCCO 34
	T2	VCCO 34
	P6	VCCO 34
	N3	VCCO 34
	K4	VCCO 34
	J1	VCCO 35
	G5	VCCO 35
	F2	VCCO 35
	D6	VCCO 35
	C3	VCCO 35
	A7	VCCO 35
		GNDADC 0

XC7A15T-1CSG324C

GND J12, A2, B5, B15, C8, C18, D1, D11, E4, E14, F7, F9, F11, F17, G8, G10, G12, H3, H7, V3, H11, H13, J6, J8, A12, J16, K7, K11, L2, L8, L12, M5, M7, M9, M11, M15, N8, N10, N12, N18, P1, R4, R14, T7, T17, U10, V13, H9

A_GND GND

U1C

ESP_RTS	R11	IO 0 14
R10	R10	IO 25 14
EPCS_MISO	K18	IO L1N T0 D01 DIN 14
EPCS_MOSI	K17	IO L1P T0 D00 MOSI 14
EPCS_HOLD	M14	IO L2N T0 D03 14
EPCS_WP	L14	IO L2P T0 D02 14
	L16	IO L3N T0 DQS EMCCLK 14
GND	L15	IO L3P T0 DQS PUDC B 14
GPIO17	M18	IO L4N T0 D05 14
GPIO18	L18	IO L4P T0 D04 14
JOY_P7	R13	IO L5N T0 D07 14
JOY_P2	R12	IO L5P T0 D06 14
KEY8_2	M13	IO L6N T0 D08 VREF 14
EPCS_CS	L13	IO L6P T0 FCS B 14
T18	T18	IO L7N T1 D10 14
GPIO2	R18	IO L7P T1 D09 14
	P14	IO L8N T1 D12 14
CPU_BUSREQ	N14	IO L8P T1 D11 14
GPIO4	P18	IO L9N T1 DQS D13 14
GPIO14	N17	IO L9P T1 DQS 14
GPIO15	M17	IO L10N T1 D15 14
KEY8_3	M16	IO L10P T1 D14 14
KEY8_1	N16	IO L11N T1 SRCC 14
GPIO10	N15	IO L11P T1 SRCC 14
R17	R17	IO L12N T1 MRCC 14
GPIO3	P17	IO L12P T1 MRCC 14
GPIO23	R15	IO L13N T2 MRCC 14
CPU_BUSACK	P15	IO L13P T2 MRCC 14
GPIO22	T15	IO L14N T2 SRCC 14
GPIO27	T14	IO L14P T2 SRCC 14
	T16	IO L15N T2 DQS DOUT CSO B 14
GPIO24	R16	IO L15P T2 DQS RDWR B 14
JOY_P3	V16	IO L16N T2 A15 D31 14
JOY_P6	V15	IO L16P T2 CSI B 14
CPU_INT_IN	U18	IO L17N T2 A13 D29 14
JOY_P4	U17	IO L17P T2 A14 D30 14
JOY_P9	V17	IO L18N T2 A11 D27 14
AUDIO_INT	U16	IO L18P T2 A12 D28 14
U11	U11	IO L19N T3 A09 D25 VREF 14
ESP_CTS	T11	IO L19P T3 A10 D26 14
ESP_RX	V12	IO L20N T3 A07 D23 14
ESP_GPIO_0	U12	IO L20P T3 A08 D24 14
I2C_SDA	V11	IO L21N T3 DQS A06 D22 14
I2C_SCL	V10	IO L21P T3 DQS 14
ESP_TX	V14	IO L22N T3 A04 D20 14
JOY_SEL	U14	IO L22P T3 A05 D21 14
ESP_GPIO_2	U13	IO L23N T3 A02 D18 14
JOY_P1	T13	IO L23P T3 A03 D19 14
T10	T10	IO L24N T3 A00 D16 14
NMI_DIVMMC	T9	IO L24P T3 A01 D17 14

XC7A15T-1CSG324C

U1D

	G13	IO 0 15
KEY8_4	K16	IO 25 15
CPU_RD	C14	IO L1N T0 AD0N 15
CPU_A10	D14	IO L1P T0 AD0P 15
CPU_A6	B14	IO L2N T0 AD8N 15
VSYNC	B13	IO L2P T0 AD8P 15
CPU_RFSH	B12	IO L3N T0 DQS AD1N 15
CPU_A3	C12	IO L3P T0 DQS AD1P 15
CPU_M1	A11	IO L4N T0 15
CPU_WR	B11	IO L4P T0 15
GPIO5	F14	IO L5N T0 AD9N 15
CPU_MREQ	F13	IO L5P T0 AD9P 15
CPU_IORQ	D13	IO L6N T0 VREF 15
CPU_A2	D12	IO L6P T0 15
CPU_IOULA	B17	IO L7N T1 AD2N 15
CPU_A8	B16	IO L7P T1 AD2P 15
CPU_A4	A16	IO L8N T1 AD10N 15
CPU_A5	A15	IO L8P T1 AD10P 15
CPU_A7	A14	IO L9N T1 DQS AD3N 15
HSYNC	A13	IO L9P T1 DQS AD3P 15
CPU_CLK3.5	A18	IO L10N T1 AD11N 15
CPU_NMI	B18	IO L10P T1 AD11P 15
GPIO13	E16	IO L11N T1 SRCC 15
GPIO19	E15	IO L11P T1 SRCC 15
CPU_A11	C15	IO L12N T1 MRCC 15
CPU_A9	D15	IO L12P T1 MRCC 15
GPIO1	G16	IO L13N T2 MRCC 15
GPIO9	H16	IO L13P T2 MRCC 15
GPIO6	F16	IO L14N T2 SRCC 15
GPIO12	F15	IO L14P T2 SRCC 15
F_DIG_D1_N	G14	IO L15N T2 DQS ADV B 15
F_DIG_D1_P	H14	IO L15P T2 DQS 15
CPU_WAIT	D17	IO L16N T2 A27 15
CPU_RAMCS	E17	IO L16P T2 A28 15
J13	J13	IO L17N T2 A25 15
KEY8_7	K13	IO L17P T2 A26 15
GPIO16	G17	IO L18N T2 A23 15
GPIO8	H17	IO L18P T2 A24 15
GPIO0	H15	IO L19N T3 A21 VREF 15
KEY8_6	J14	IO L19P T3 A22 15
CPU_HALT	C17	IO L20N T3 A19 15
CPU_INT	C16	IO L20P T3 A20 15
CPU_ROMCS	D18	IO L21N T3 DQS A18 15
GPIO20	E18	IO L21P T3 DQS 15
GPIO26	F18	IO L22N T3 A16 15
GPIO7	G18	IO L22P T3 A17 15
GPIO25	J18	IO L23N T3 FWE B 15
GPIO11	J17	IO L23P T3 FOE B 15
KEY8_8	J15	IO L24N T3 RS0 15
KEY8_5	K15	IO L24P T3 RS1 15

XC7A15T-1CSG324C

U1F

	K6	IO 0 34
CPU_RST	U8	IO 25 34
SD_SCK	M1	IO L1N T0 34
SD_MISO	L1	IO L1P T0 34
PS2_PIN2	L3	IO L2N T0 34
VID_R2	K3	IO L2P T0 34
SD_CS	N1	IO L3N T0 DQS 34
RAM_A7	N2	IO L3P T0 DQS 34
SD_MOSI	M2	IO L4N T0 34
RAM_D7	M3	IO L4P T0 34
PS2_DATA	L4	IO L5N T0 34
VID_R1	K5	IO L5P T0 34
PS2_PIN6	L5	IO L6N T0 VREF 34
	L6	IO L6P T0 34
RAM_D5	V1	IO L7N T1 34
RAM_D4	U1	IO L7P T1 34
RAM_D15	U3	IO L8N T1 34
	U4	IO L8P T1 34
RAM_A18	V2	IO L9N T1 DQS 34
RAM_D6	U2	IO L9P T1 DQS 34
	V4	IO L10N T1 34
MIC_PORT	V5	IO L10P T1 34
RAM_A8	T3	IO L11N T1 SRCC 34
RAM_A9	R3	IO L11P T1 SRCC 34
	T4	IO L12N T1 MRCC 34
CLK	T5	IO L12P T1 MRCC 34
RAM_A12	P5	IO L13N T2 MRCC 34
	N5	IO L13P T2 MRCC 34
RAM_A13	P3	IO L14N T2 SRCC 34
RAM_A10	P4	IO L14P T2 SRCC 34
RAM_A16	R2	IO L15N T2 DQS 34
RAM_A17	P2	IO L15P T2 DQS 34
RAM_A11	N4	IO L16N T2 34
RAM_WE	M4	IO L16P T2 34
RAM_A15	T1	IO L17N T2 34
RAM_A14	R1	IO L17P T2 34
	N6	IO L18N T2 34
	M6	IO L18P T2 34
RAM_A19	R5	IO L19N T3 VREF 34
	R6	IO L19P T3 34
RAM_D13	V6	IO L20N T3 34
KEY5_2	V7	IO L20P T3 34
BT_RST	V9	IO L21N T3 DQS 34
RAM_D12	U9	IO L21P T3 DQS 34
KEY5_1	U6	IO L22N T3 34
RAM_D14	U7	IO L22P T3 34
KEY5_3	T6	IO L23N T3 34
KEY5_4	R7	IO L23P T3 34
NMI_MULTI	T8	IO L24N T3 34
KEY5_5	R8	IO L24P T3 34

XC7A15T-1CSG324C

U1G

RAM_LB	F5	IO 0 35
VID_R0	J5	IO 25 35
CPU_D1	C5	IO L1N T0 AD4N 35
CPU_D2	C6	IO L1P T0 AD4P 35
EAR_PORT	B6	IO L2N T0 AD12N 35
GPIO21	B7	IO L2P T0 AD12P 35
RAM_D9	A5	IO L3N T0 DQS AD5N 35
RAM_D11	A6	IO L3P T0 DQS AD5P 35
CPU_D5	C7	IO L4N T0 35
CPU_D3	D8	IO L4P T0 35
F_DIG_D0_N	E5	IO L5N T0 AD13N 35
F_DIG_D0_P	E6	IO L5P T0 AD13P 35
CPU_D6	D7	IO L6N T0 VREF 35
CPU_Y	E7	IO L6P T0 35
AUDIO_L	B4	IO L7N T1 AD6N 35
CPU_D7	C4	IO L7P T1 AD6P 35
VID_B0	A3	IO L8N T1 AD14N 35
AUDIO_R	A4	IO L8P T1 AD14P 35
AD7N	A1	IO L9N T1 DQS AD7N 35
AD7P	B1	IO L9P T1 DQS AD7P 35
AD15N	B2	IO L10N T1 AD15N 35
AD15P	B3	IO L10P T1 AD15P 35
RAM_D10	D4	IO L11N T1 SRCC 35
CPU_D0	D5	IO L11P T1 SRCC 35
RAM_D8	D3	IO L12N T1 MRCC 35
RAM_UB	E3	IO L12P T1 MRCC 35
RAM_A3	F3	IO L13N T2 MRCC 35
RAM_OE	F4	IO L13P T2 MRCC 35
RAM_A1	D2	IO L14N T2 SRCC 35
RAM_A4	E2	IO L14P T2 SRCC 35
RAM_D0	G2	IO L15N T2 DQS 35
RAM_D2	H2	IO L15P T2 DQS 35
RAM_A0	C1	IO L16N T2 35
VID_B1	C2	IO L16P T2 35
RAM_D1	G1	IO L17N T2 35
RAM_D3	H1	IO L17P T2 35
RAM_A2	E1	IO L18N T2 35
RAM_CS	F1	IO L18P T2 35
	F6	IO L19N T3 VREF 35
	G6	IO L19P T3 35
VID_B2	G3	IO L20N T3 35
RAM_A5	G4	IO L20P T3 35
VID_G0	H4	IO L21N T3 DQS 35
VID_G1	J4	IO L21P T3 DQS 35
RAM_A6	J2	IO L22N T3 35
VID_G2	J3	IO L22P T3 35
PS2_CLK	K1	IO L23N T3 35
SD_CS2	K2	IO L23P T3 35
F_DIG_D2_N	H5	IO L24N T3 35
F_DIG_D2_P	H6	IO L24P T3 35

XC7A15T-1CSG324C

U1A

+3.3V

R140 0402 1% 330R (DNF)

R136 0402 1% 4.7k

P9

DONE_0

GND

	P12	M0 0
	P13	M1 0
	P11	M2 0
	P7	INIT 0
	P9	PROGRAM 0
	P8	CFGBVS 0
	P10	DONE 0
	L9	DXN 0
	L10	DXP 0
TAPE_N	K9	VN 0
TAPE_P	J10	VP 0
TCK	E10	TCK 0
TDI	E11	TDI 0
TDO	E13	TDO 0
TMS	E12	TMS 0
EPCS_SCK	E9	CCLK 0

XC7A15T-1CSG324C

U1E

EPCS_SCK	D9	IO L6N T0 VREF 16
CPU_A13	B9	IO L11N T1 SRCC 16
CPU_D4	C9	IO L11P T1 SRCC 16
CPU_A15	A8	IO L12N T1 MRCC 16
CPU_A14	B8	IO L12P T1 MRCC 16
F_DIG_CLK_N	C10	IO L13N T2 MRCC 16
F_DIG_CLK_P	C11	IO L13P T2 MRCC 16
CPU_A12	A9	IO L14N T2 SRCC 16
CPU_A0	A10	IO L14P T2 SRCC 16
CPU_A1	D10	IO L19N T3 VREF 16

XC7A15T-1CSG324C

Clock

+3.3V

R103 120R 1% 0402

C135 X5R 0402 1uF 16V

C25 X5R 0402 1uF 16V

GND

Y2 ECS-2520MV-500 50MHz (VDD, OUT, GND, CTRL)

R102 47R 1% 0402 CLK

JTAG header

JTAG T821114A1S100CEU

TDI, TDO, TCK, TMS, +3.3V, GND

Jumper

+3.3V

R1 4.7k 1% 0402

J19 M20-9990246

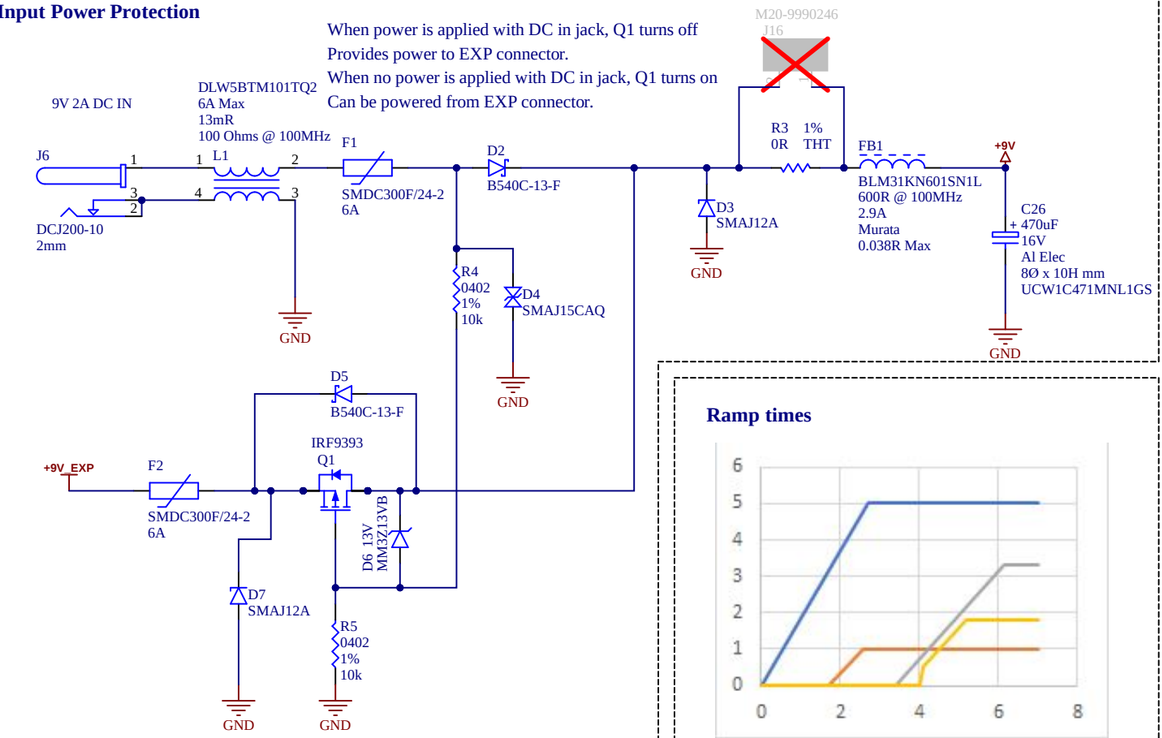
P9

GND

SpectrumNext			SpecNext Ltd
FPGA			
Drawn By:			
Project #: PR0064	Rev: 3.4	Variant : V3	Sheet: 2 of 8

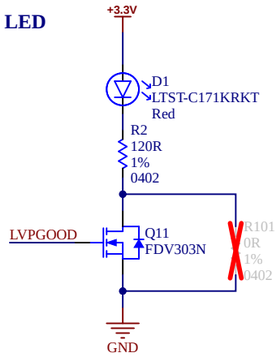
Input Power Protection

When power is applied with DC in jack, Q1 turns off
Provides power to EXP connector.
When no power is applied with DC in jack, Q1 turns on
Can be powered from EXP connector.

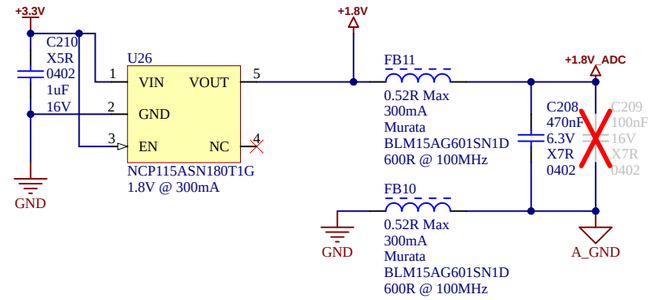


Ramp times

Power LED



1.8V LDO

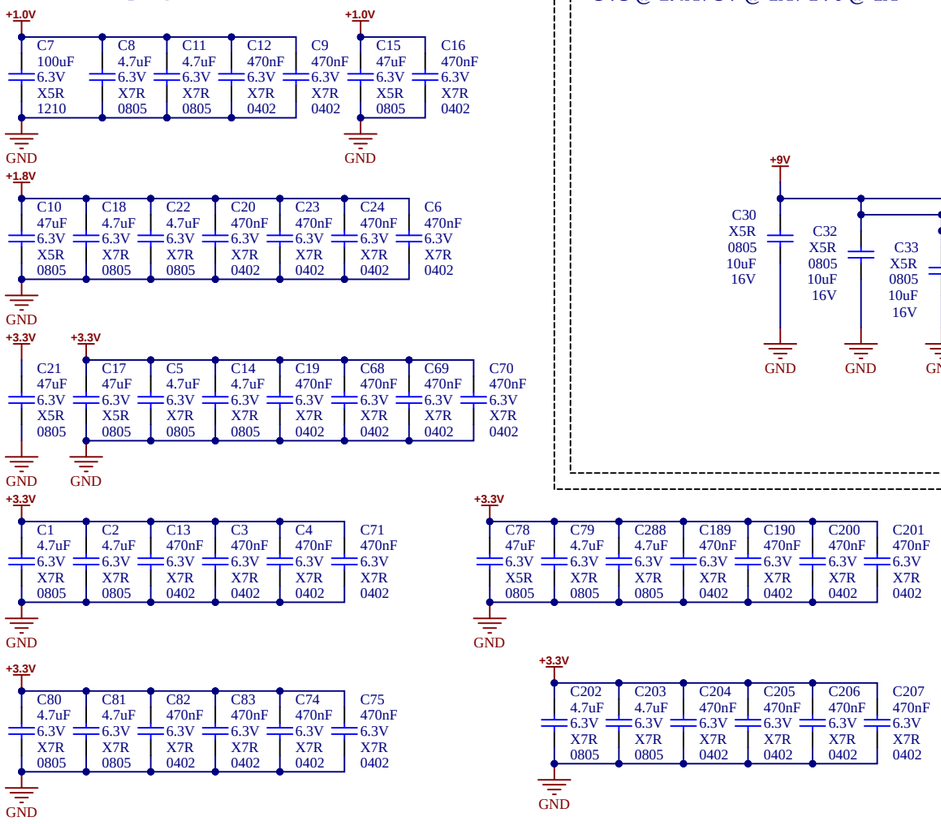


U8 Power Sequencing

Table 2. Power Sequencing

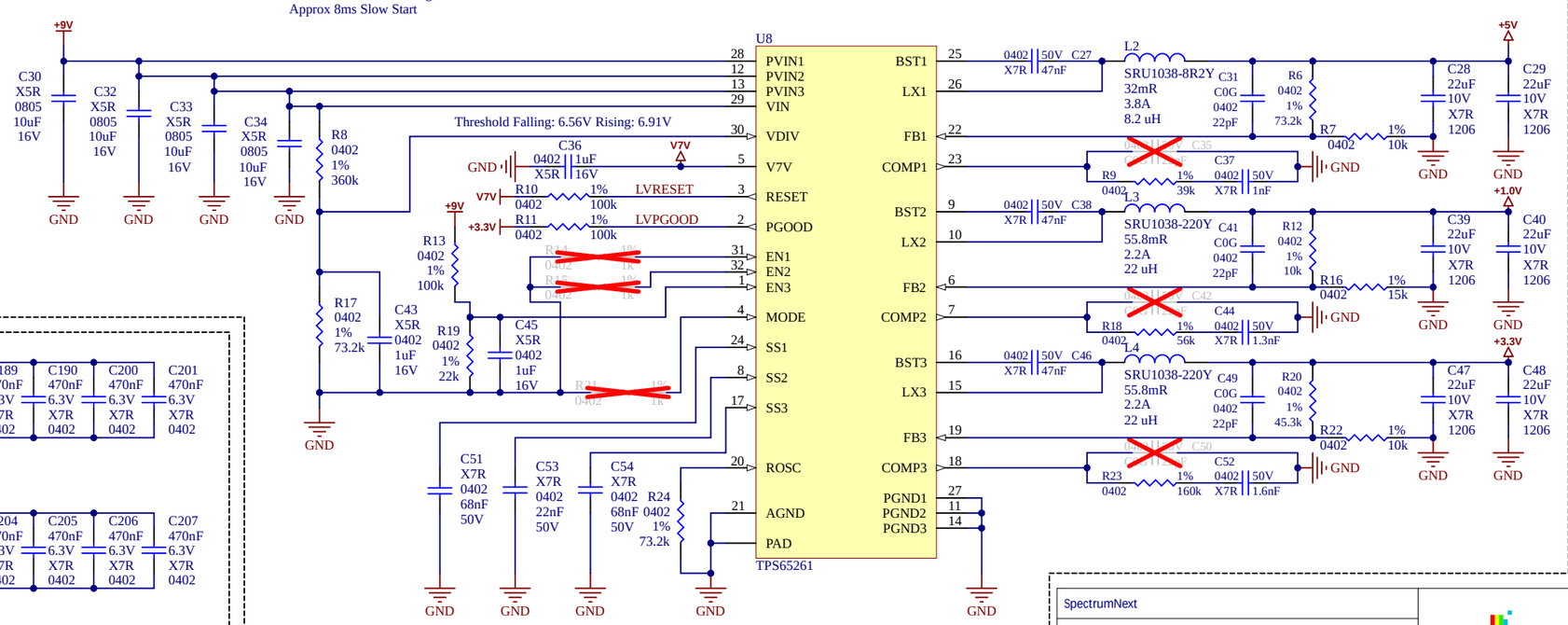
	MODE	EN1	EN2	EN3	Start Sequencing	Shutdown Sequencing
Automatic Power Sequencing	High	High	High	Used to start/stop bucks in sequence	Buck1→Buck2→Buck3	Buck3→Buck2→Buck1
	High	Low	High		Buck2→Buck1→Buck3	Buck3→Buck1→Buck2
	High	High	Low		Buck2→Buck3→Buck1	Buck1→Buck3→Buck2
	High	Low	Low	Reserved	Reserved	Reserved
Externally controlled sequencing	Low	Used to start/stop buck1	Used to start/stop buck2	Used to start/stop buck3	x	x

FPGA Decoupling

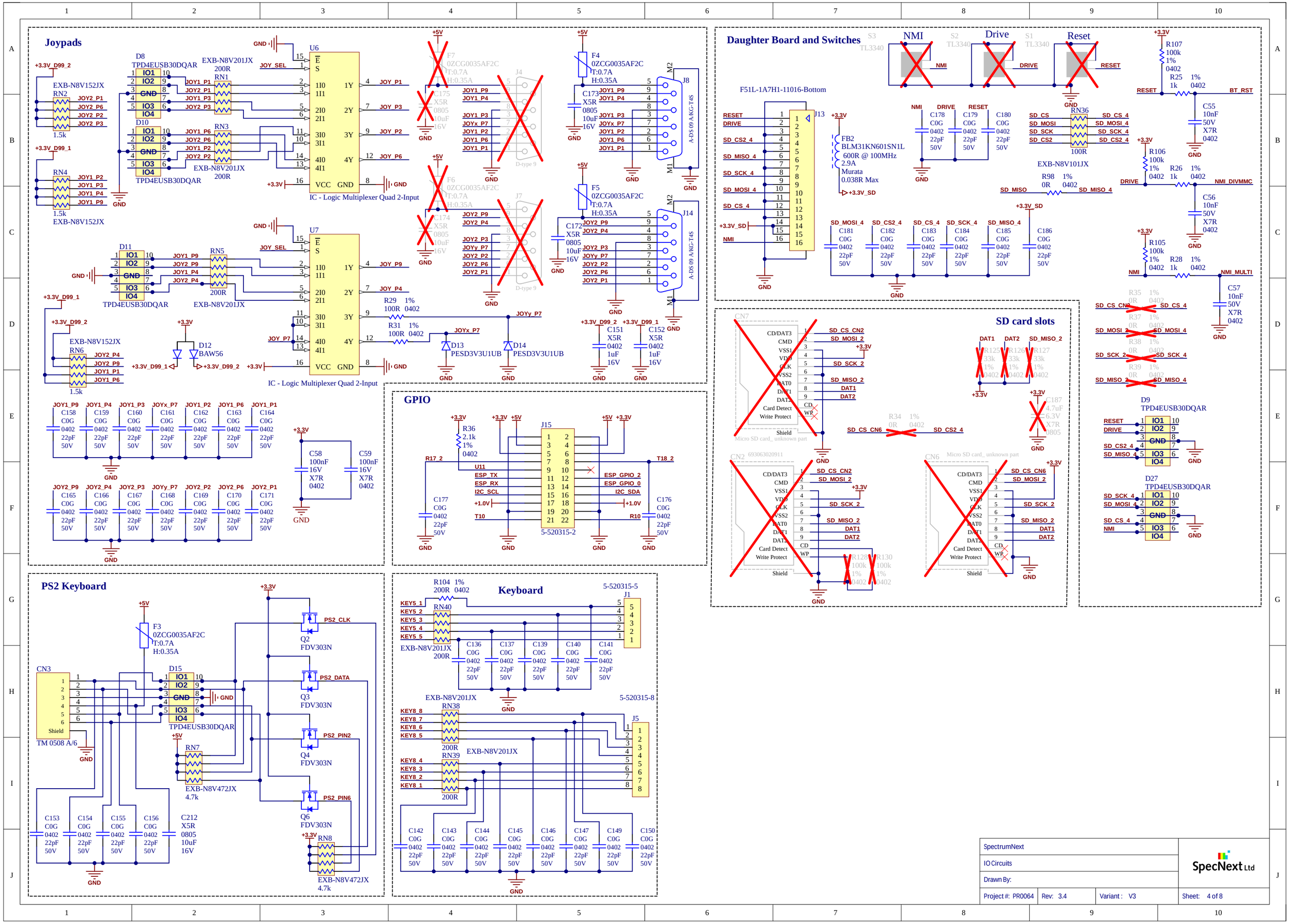


3V3 @ 2.4A / 5V @ 1A / 1V0 @ 1A

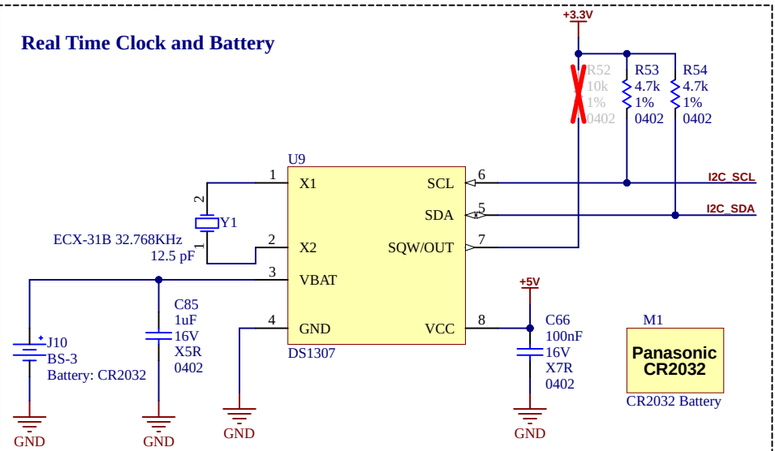
EN1 + EN2 High, Buck1->Buck2->Buck3 startup
START 5V first due to logic buffers
Approx 8ms Slow Start



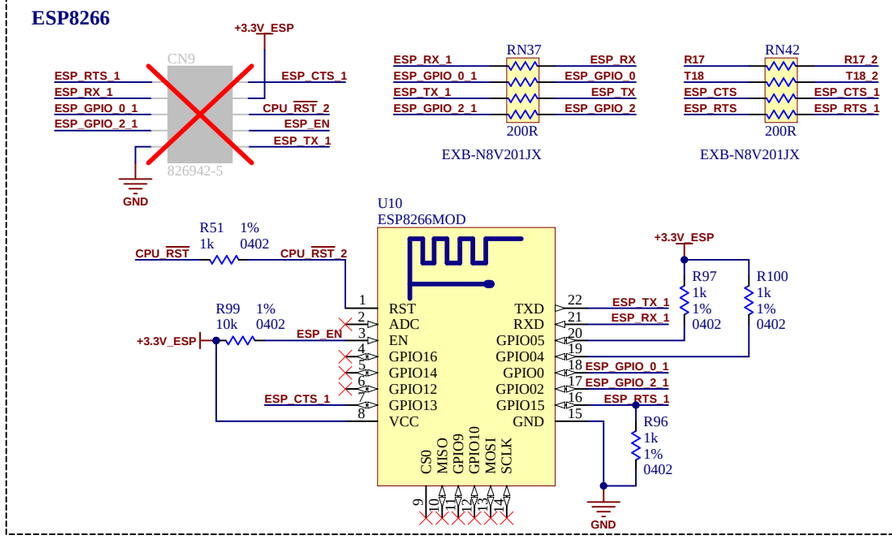
SpectrumNext			SpecNext Ltd
Power Supply			
Drawn By:			
Project #: PR0064	Rev: 3.4	Variant : V3	Sheet: 3 of 8


Joypads
Daughter Board and Switches
SD card slots
GPIO
PS2 Keyboard
Keyboard
IC - Logic Multiplexer Quad 2-Input
IC - Logic Multiplexer Quad 2-Input
NMI
Drive
Reset
F51L-1A7H1-11016-Bottom
EXB-N8V101JX
EXB-N8V152JX
EXB-N8V201JX
EXB-N8V472JX
TPD4EUSB30DQAR
TM 0508 A/6
5-520315-2
5-520315-5
5-520315-8
A-DS 09 A/KG-T4S
D-type 9
Micro SD card_ unknown part
SpectrumNext
IO Circuits
Drawn By:
Project #: PR0064
Rev: 3.4
Variant : V3
Sheet: 4 of 8
SpecNext Ltd

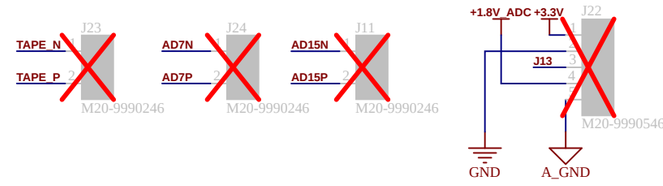
Real Time Clock and Battery



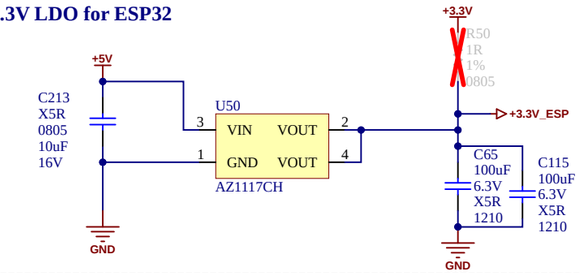
ESP8266



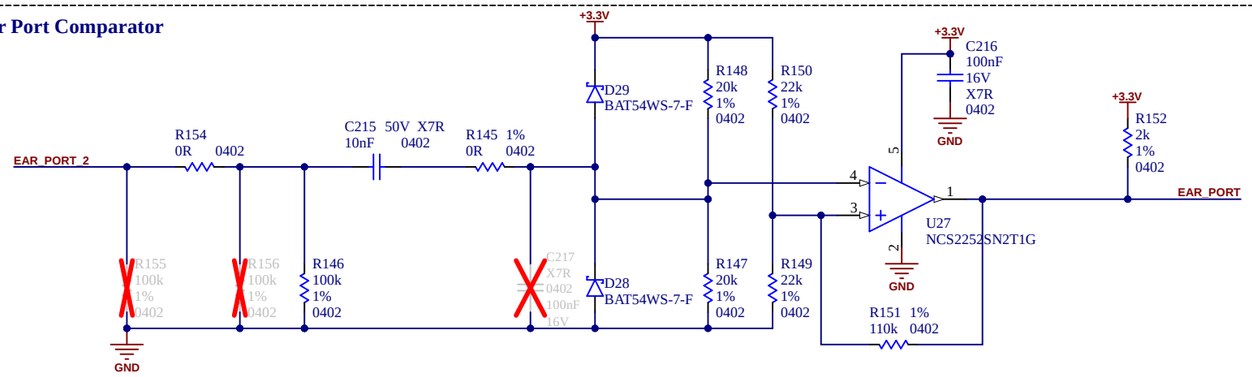
FPGA A2D headers



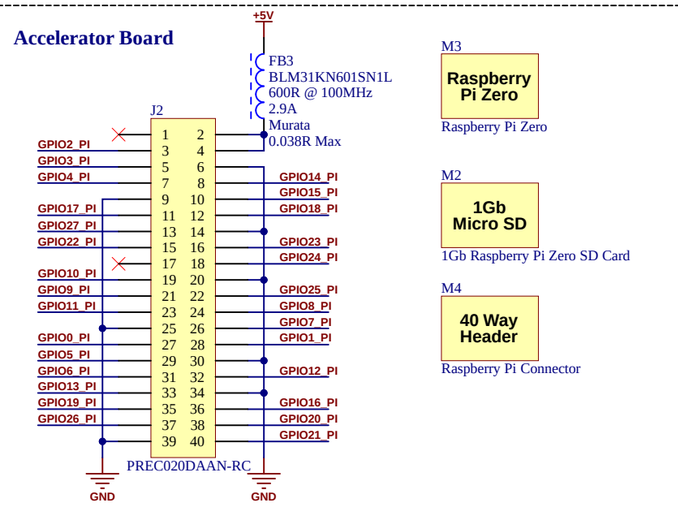
3.3V LDO for ESP32



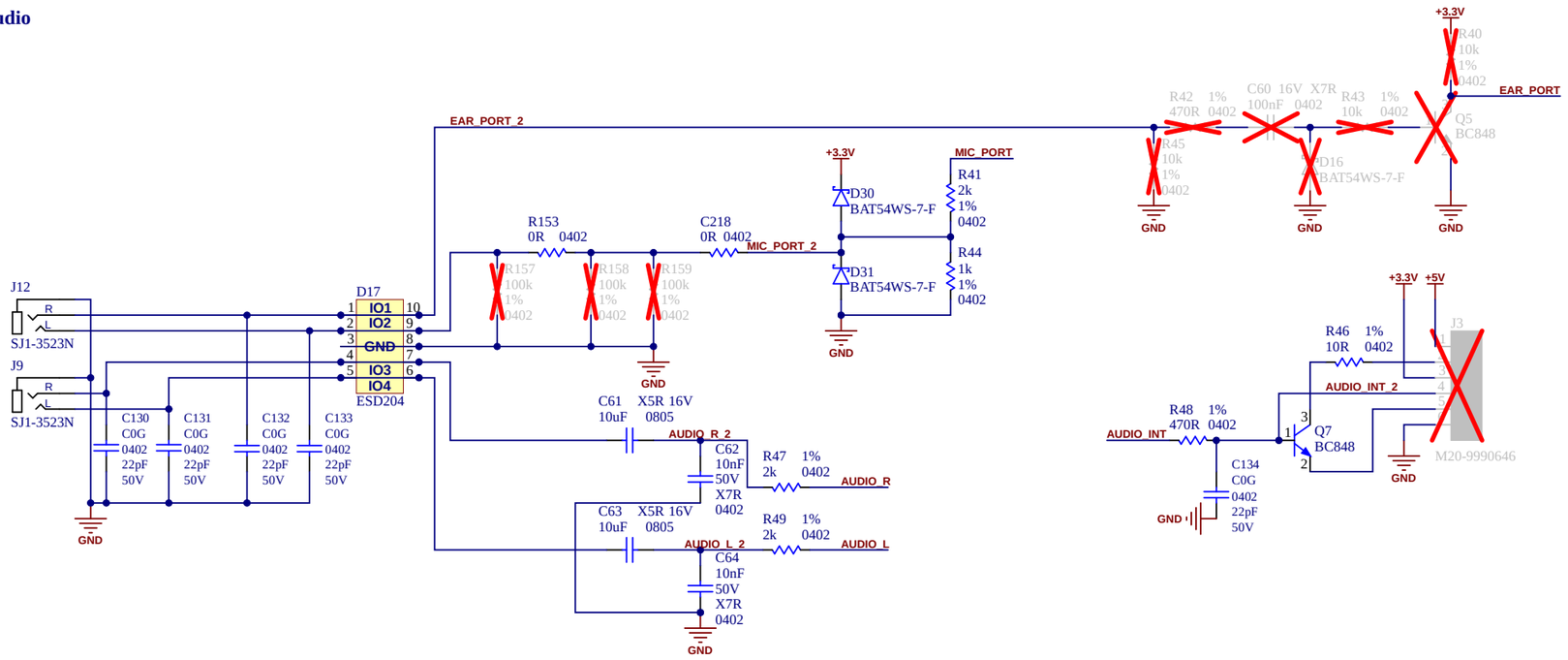
Ear Port Comparator



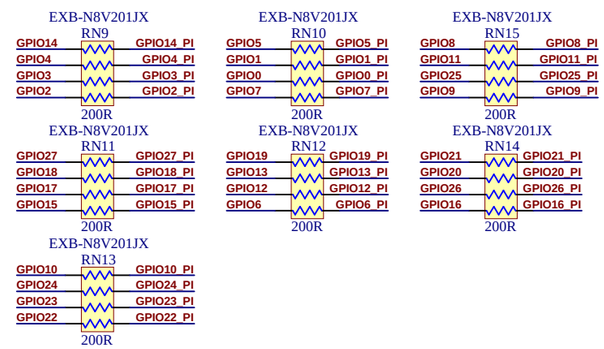
Accelerator Board



Audio

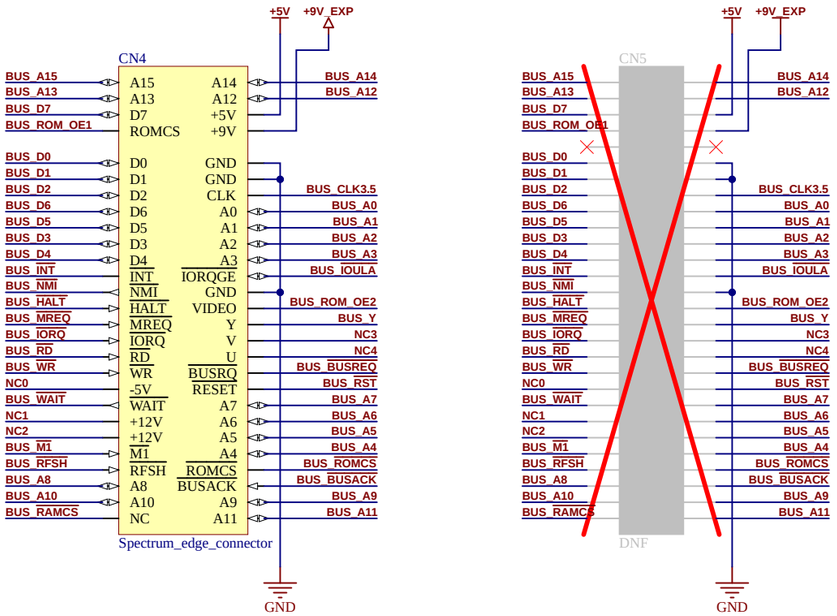


Raspberry Pi GPIO resistors

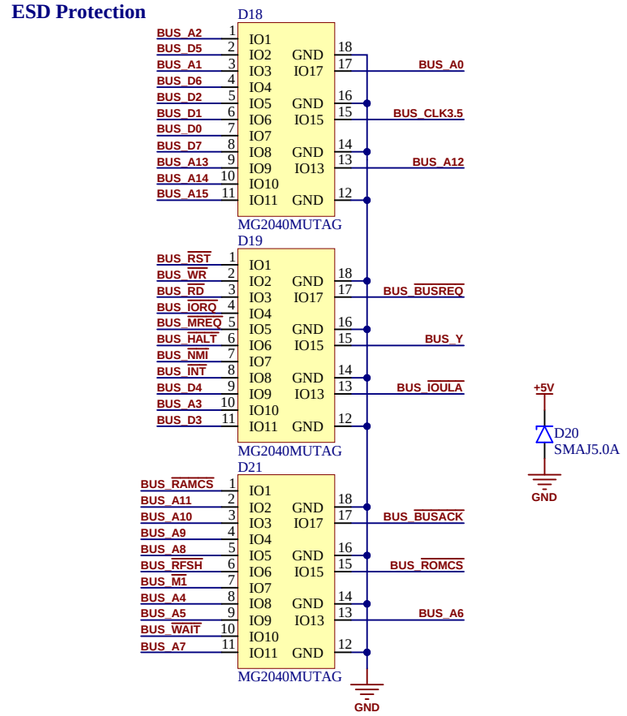


SpectrumNext			SpecNext Ltd
Peripherals			
Drawn By:			
Project #: PR0064	Rev: 3.4	Variant : V3	Sheet: 5 of 8

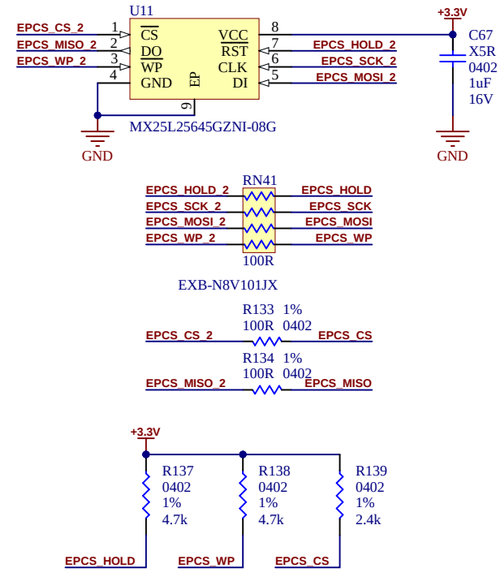
Spectrum Edge Connector



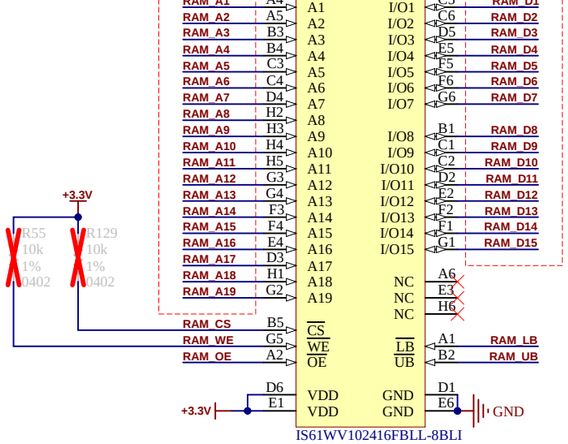
ESD Protection



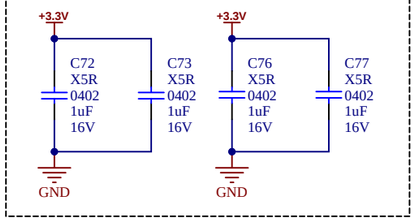
Flash memory



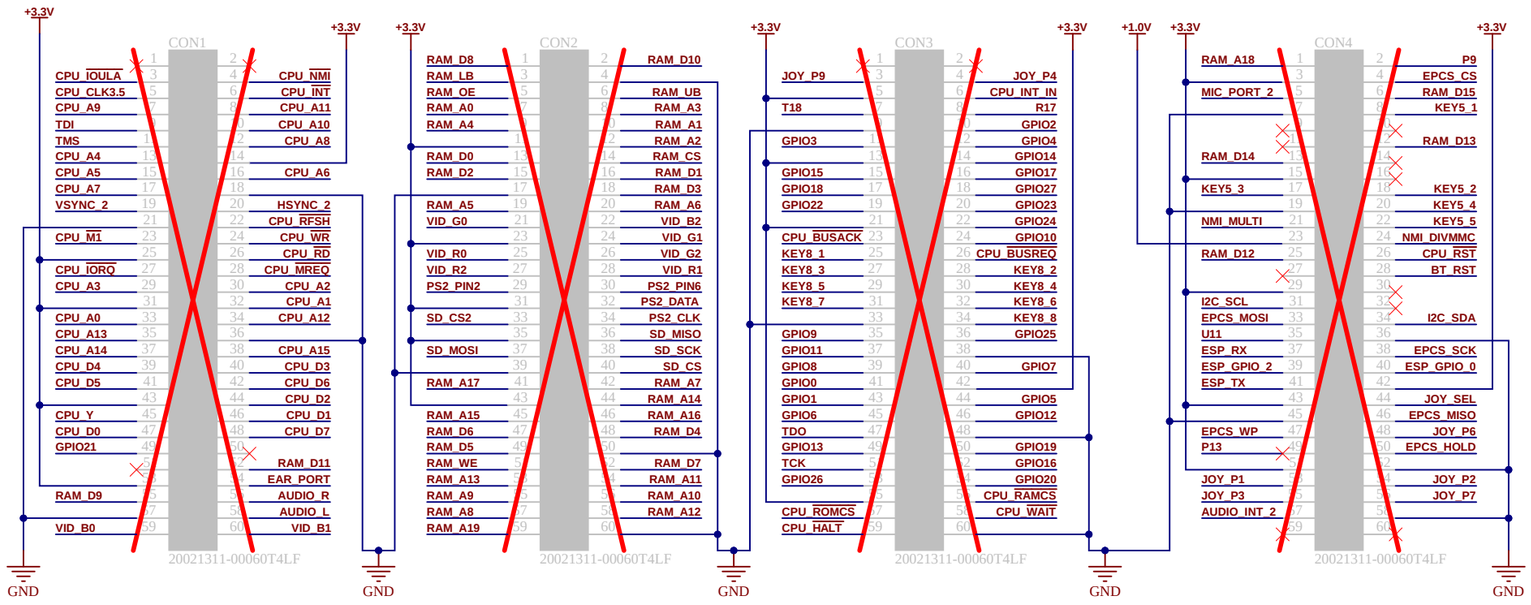
SRAM



SRAM Decoupling

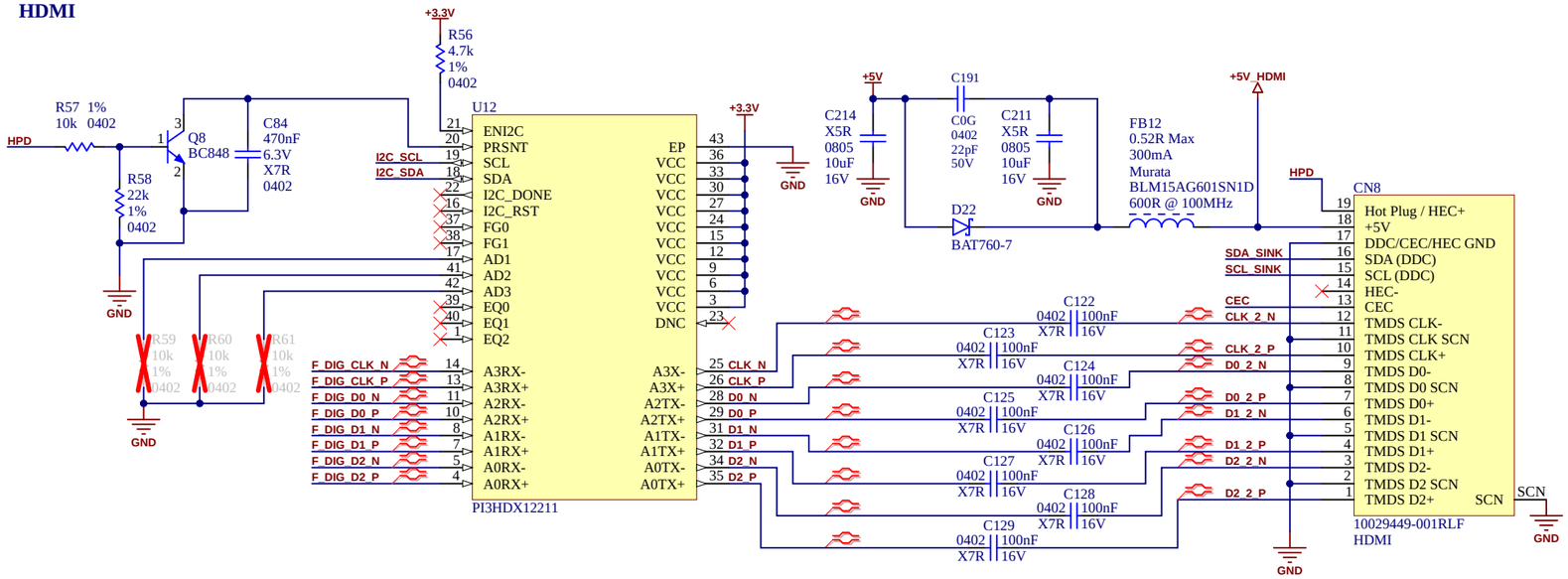


Test Point Headers

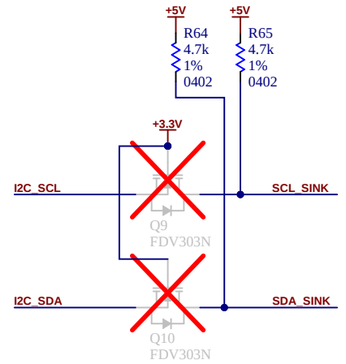


SpectrumNext	SpecNext Ltd
Memory Expansion	
Drawn By:	
Project #: PR0064 · Rev: 3.4 · Variant : V3	Sheet: 6 of 8

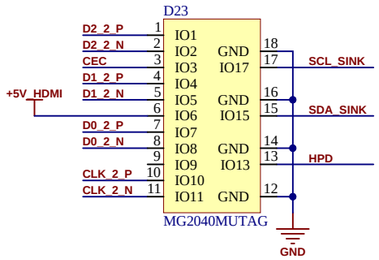
HDMI



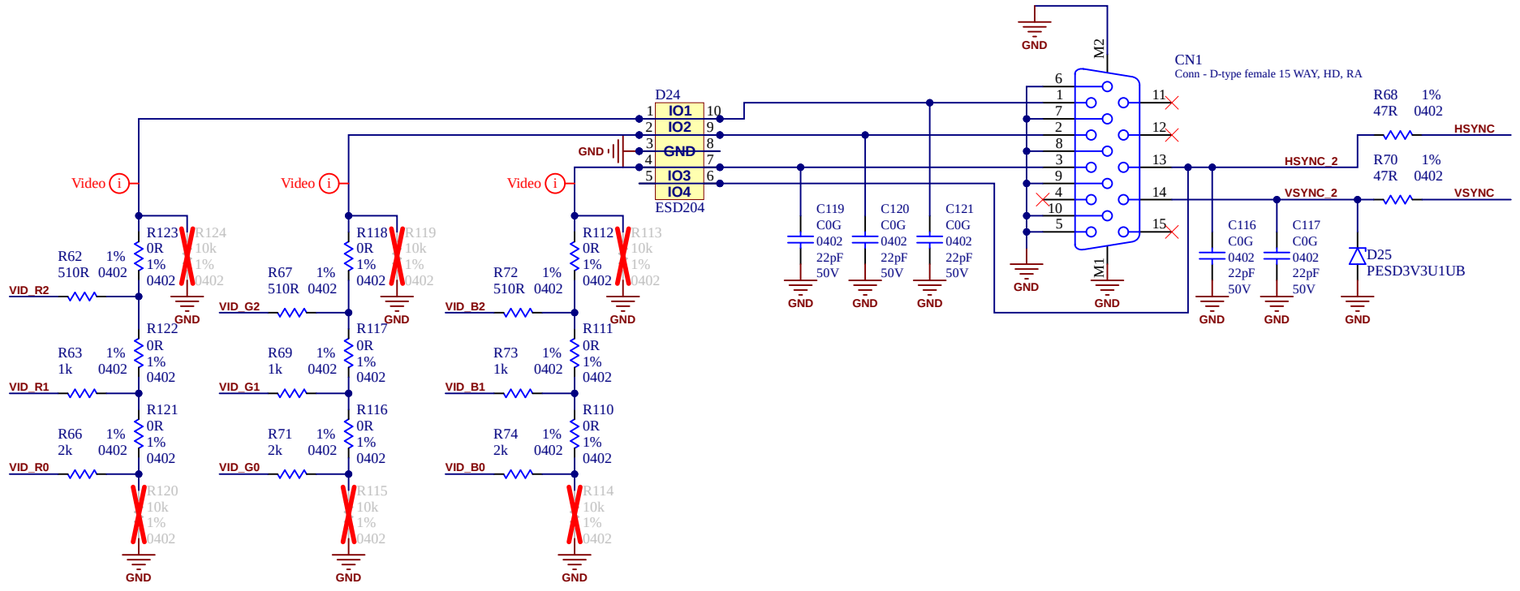
I2C level conversion for HDMI EEPROM



HDMI ESD

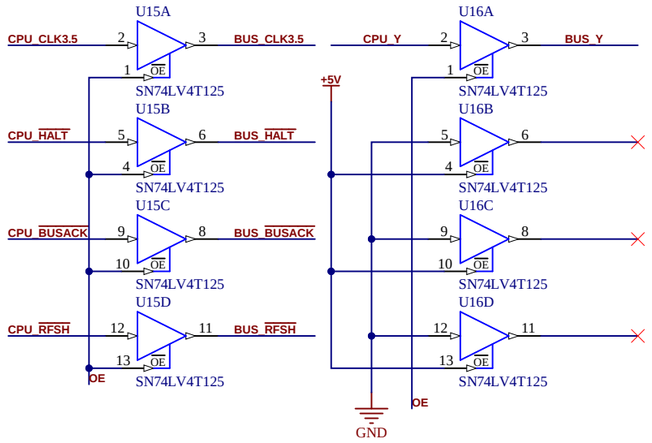


VGA

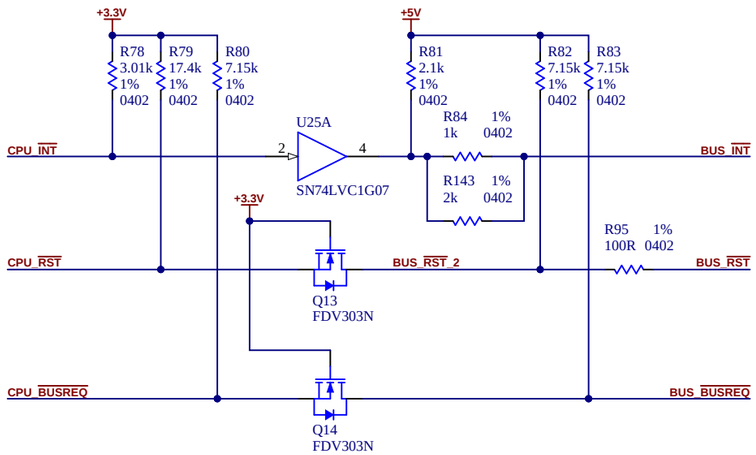


SpectrumNext			SpecNext Ltd
Displays			
Drawn By:			
Project #: PR0064	Rev: 3.4	Variant : V3	Sheet: 7 of 8

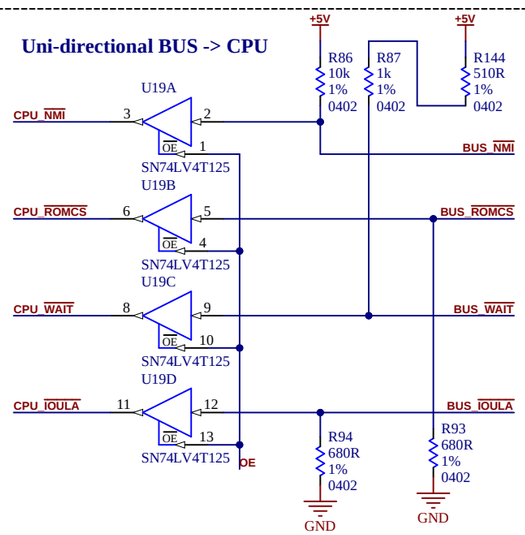
Uni-directional CPU -> BUS



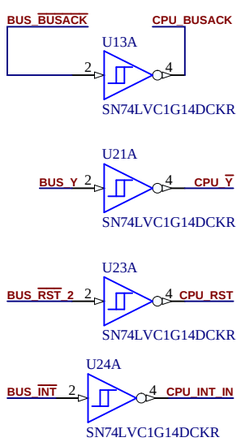
Open Drain



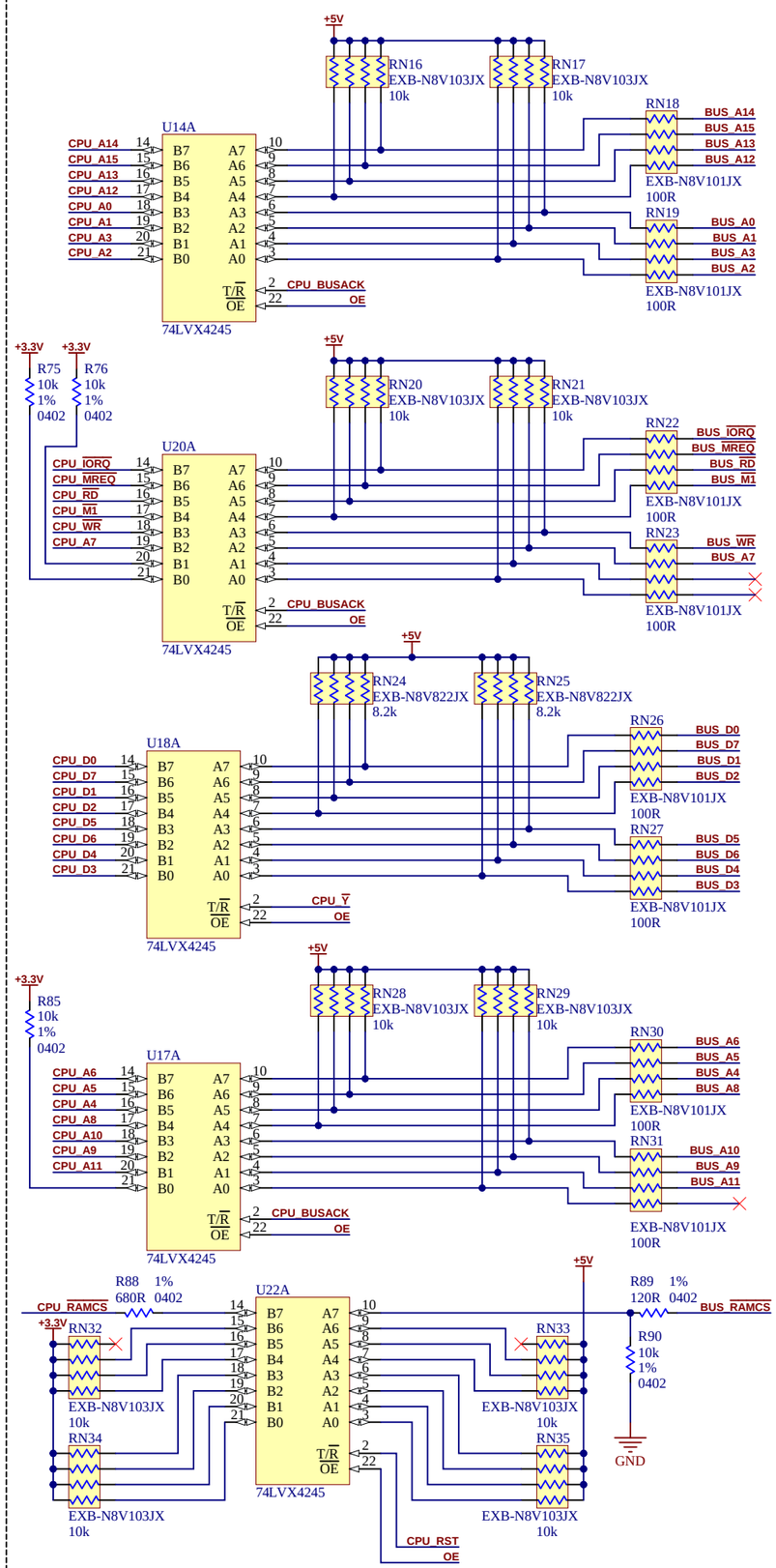
Uni-directional BUS -> CPU



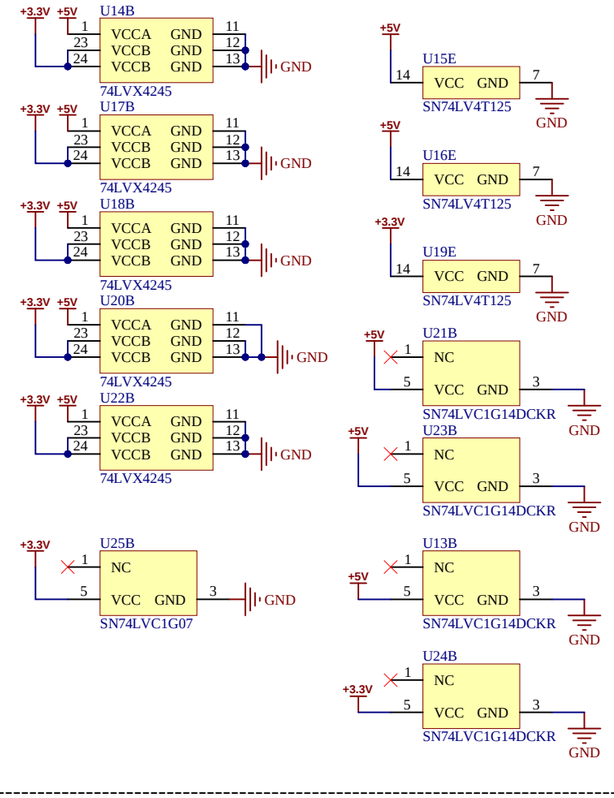
Direction Control



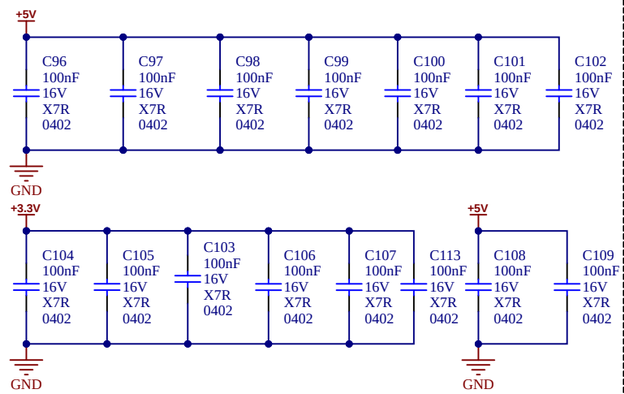
Bi-directional



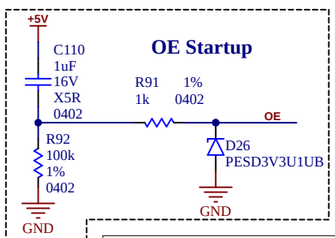
Power

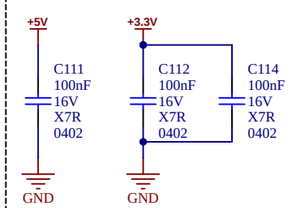


Decoupling



OE Startup





SpectrumNext			SpecNext Ltd
Expansion Buffers			
Drawn By:			
Project #: PR0064	Rev: 3.4	Variant : V3	Sheet: 8 of 8